FIG.1

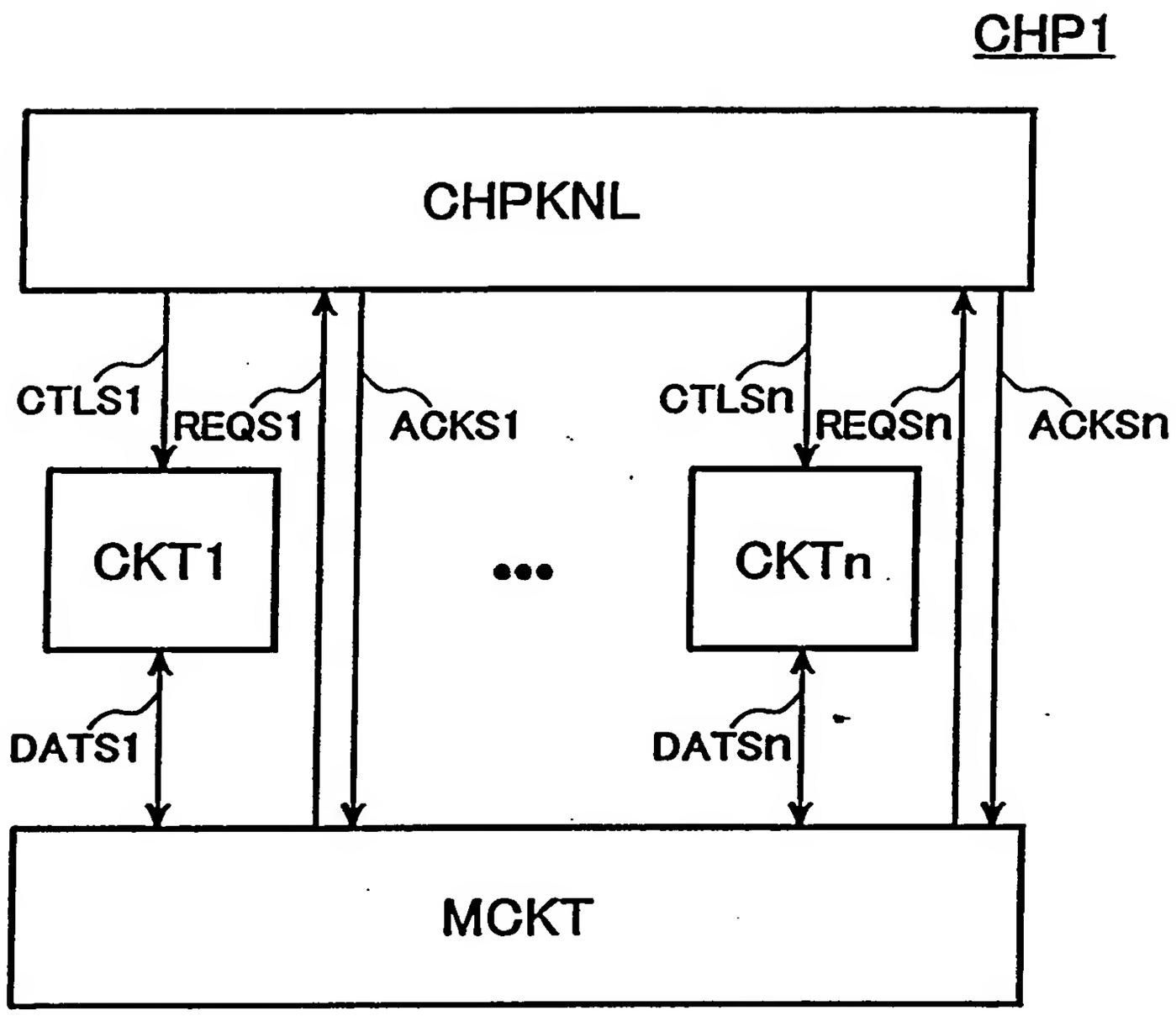
CHP1
CHPKNL
CTLS1
REQS1
ACKS1
CTLSn
REQSn
ACKSn
CKT1
CKTn
DATS1
DATSn
MCKT

FIG.2

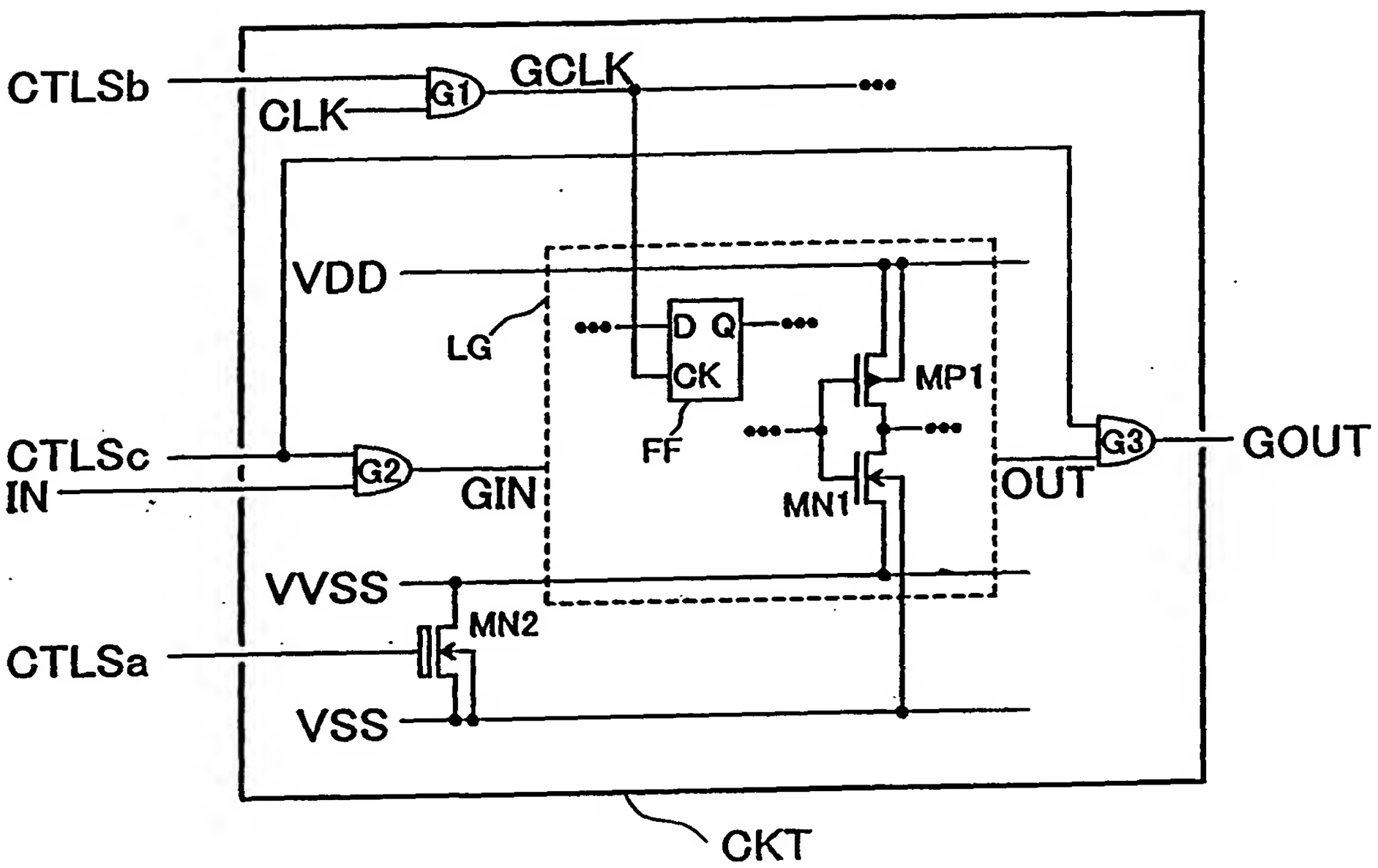
CTLSb
CLK
G1
GCLK
VDD
LG
D Q
CK
FF
MP1
MN1
CTLSc
IN
G2
GIN
OUT
G3
GOUT
VVSS
MN2
CTLSa
VSS
CKT

FIG.3

	ACT	STB	SLP
CKT1 (CPU)	50mW	20mW	0mW
CKT2 (FPU)	100mW	50mW	0mW
CKT3 (DSP)	30mW	10mW	0mW
CKT4 (RF)	150mW	0mW	0mW

FIG.4

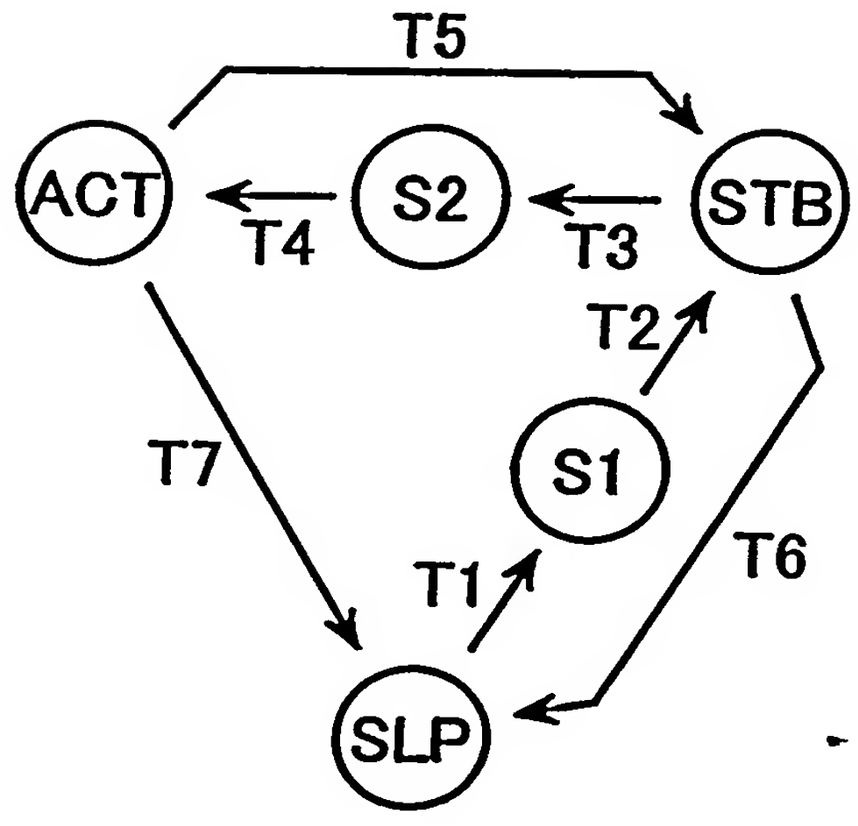

FIG.5

TIME	CKT1 (CPU)	CKT2 (FPU)	CKT3 (DSP)	CKT4 (RF)	PWR
0		STB	SLP		100mW
1	ACT	ACT			150mW
2			STB	STB	60mW
3	SLP	SLP			30mW
4			ACT		30mW
5	STB			ACT	200mW
6	ACT	STB	STB	STB	110mW

FIG.6

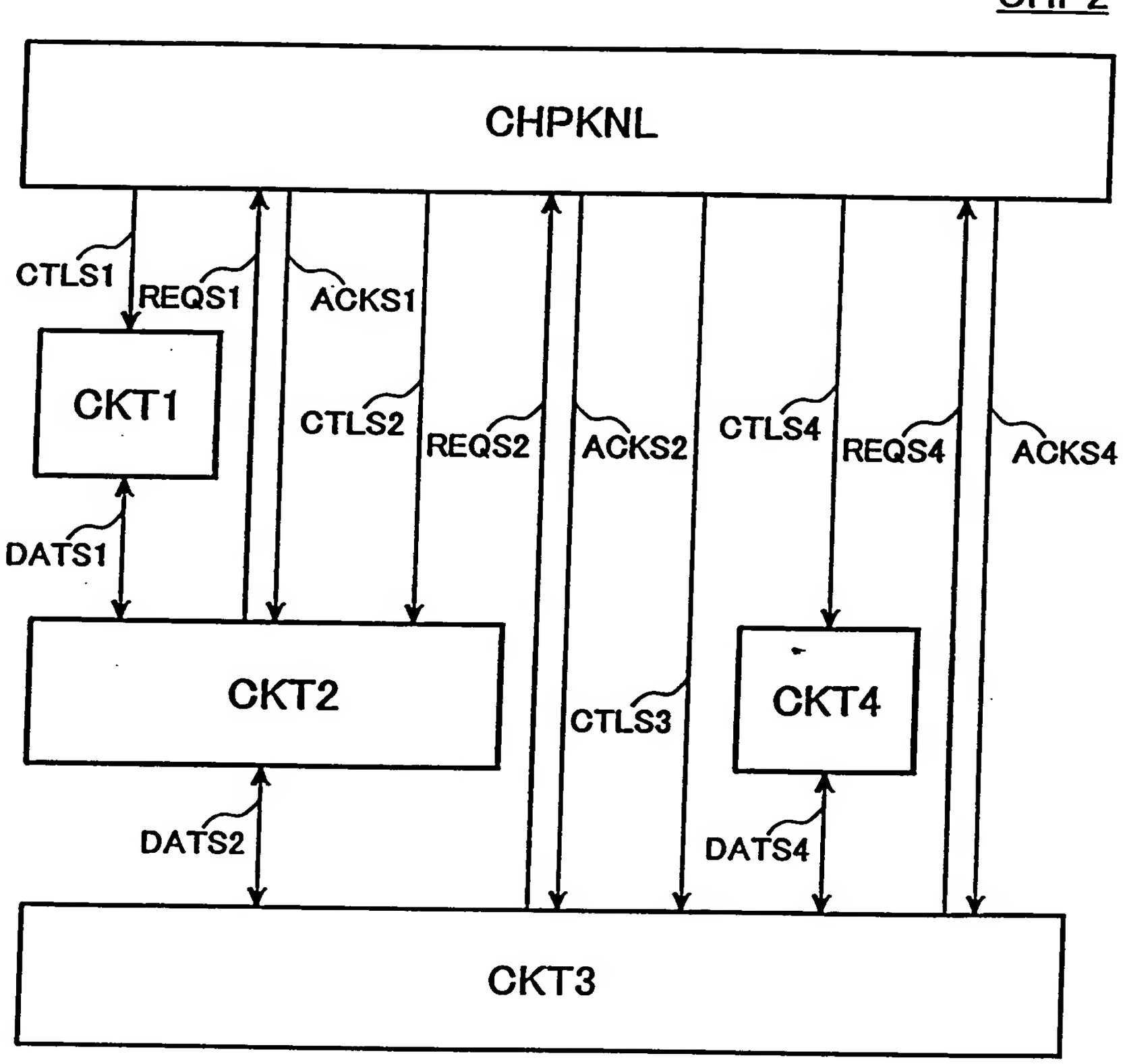
CHP2
CHPKNL
CTLS1
REQS1
ACKS1
CKT1
CTLS2
REQS2
ACKS2
CTLS4
REQS4
ACKS4
DATS1
CKT2
CTLS3
CKT4
DATS2
DATS4
CKT3

FIG.7

TIME	CKT1 (CPU)	CKT2 (FPU)	CKT3 (DSP)	CKT4 (RF)	PWR
0	ACT	STB	SLP	STB	100mW
1	ACT	ACT	SLP	STB	150mW
2	ACT	ACT	STB	STB	60mW
3	SLP	SLP	STB	STB	30mW
4	SLP	SLP	ACT	STB	30mW
5	STB	SLP	SLP	STB	50mW
6	SLP	SLP	SLP	ACT	150mW

FIG.8

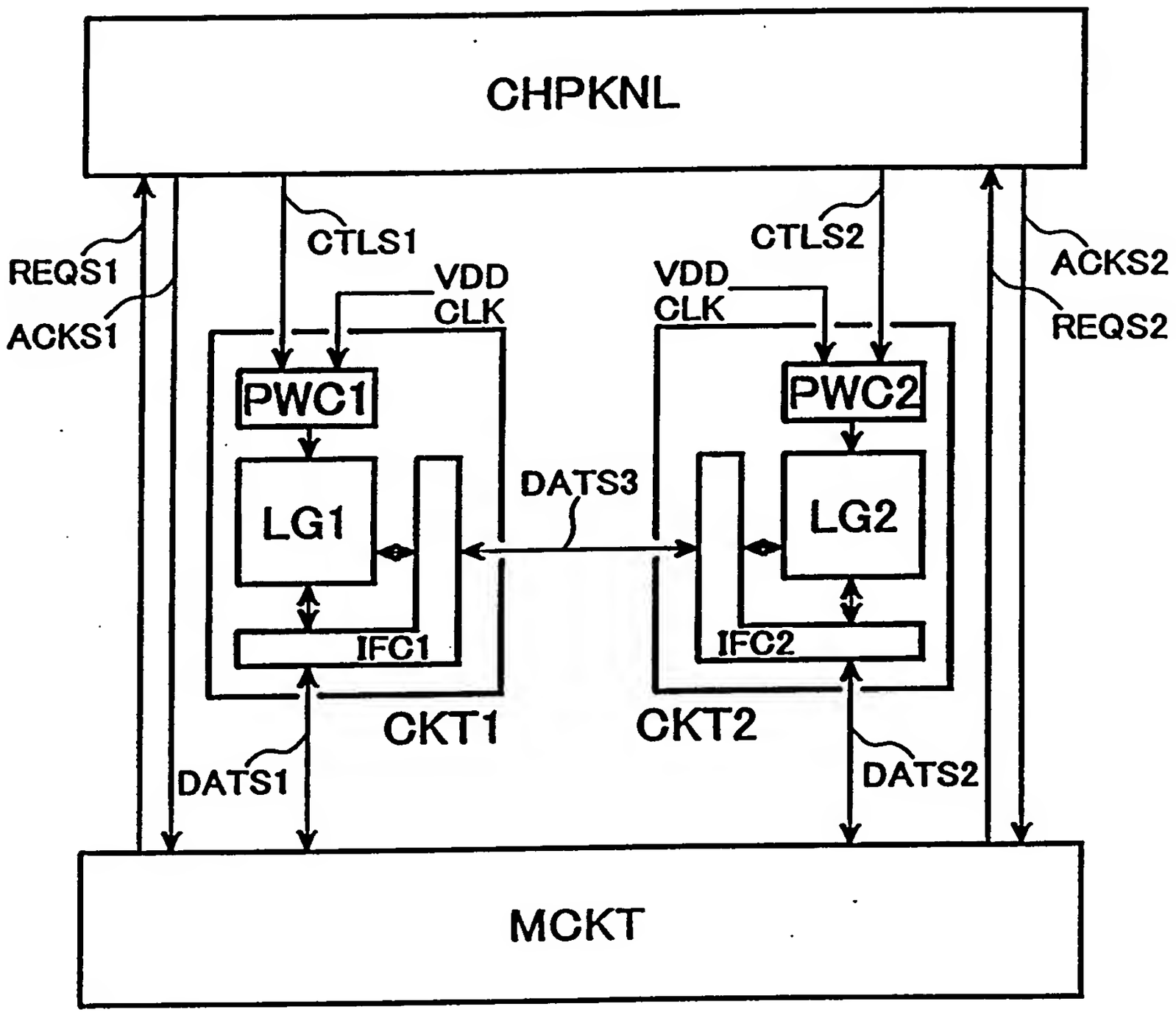
CHP3
CHPKNL
REQS1
ACKS1
CTLS1
VDD
CLK
PWC1
LG1
IFC1
CKT1
DATS3
CTLS2
VDD
CLK
PWC2
LG2
IFC2
CKT2
ACKS2
REQS2
DATS1
DATS2
MCKT

FIG.9

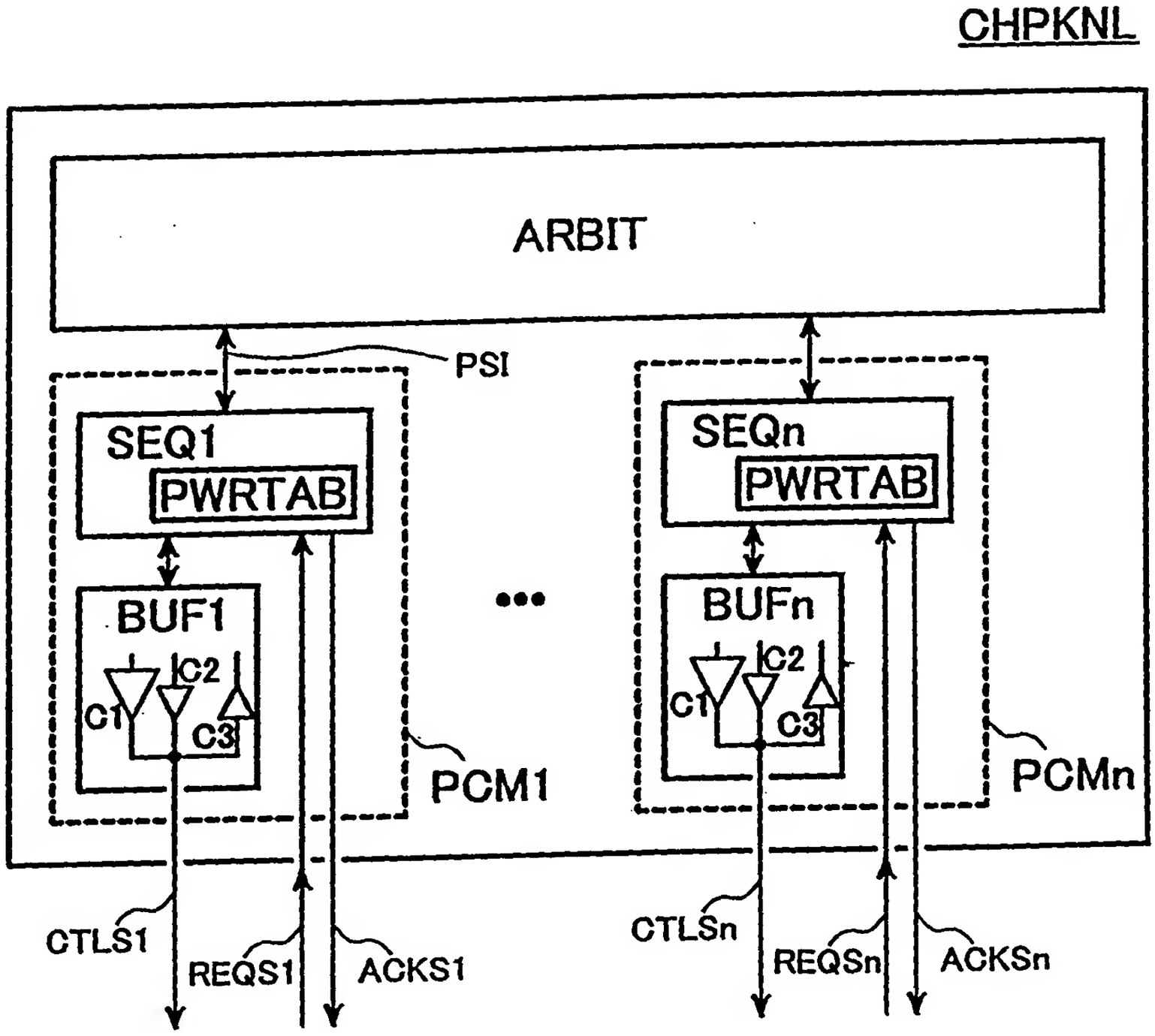
CHPKNL
ARBIT
PSI
SEQ1
PWRTAB
BUF1
C1
C2
C3
PCM1
SEQn
PWRTAB
BUFn
C1
C2
C3
PCMn
CTLS1
REQS1
ACKS1
CTLSn
REQSn
ACKSn

FIG.10

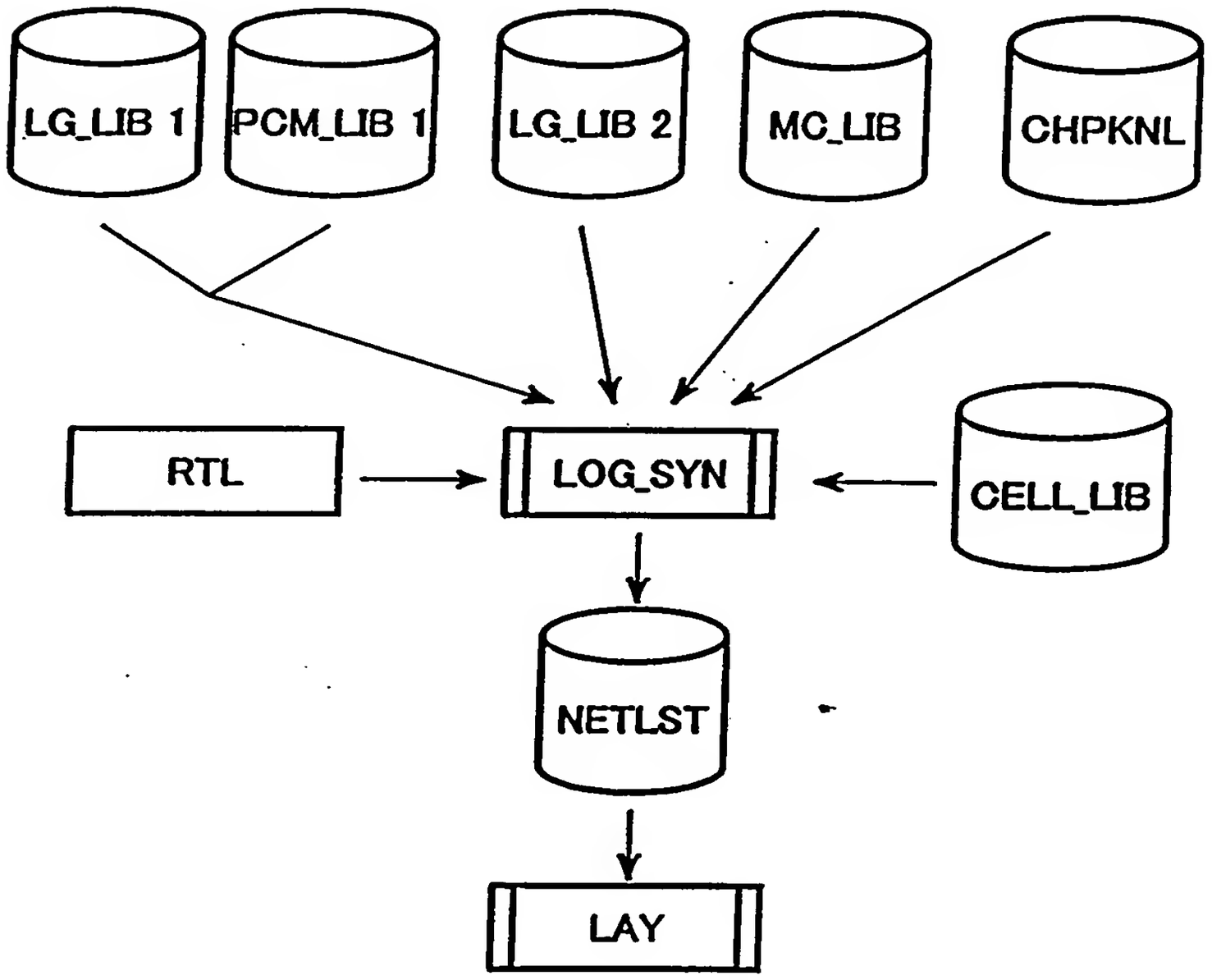
LG_LIB 1
PCM_LIB 1
LG_LIB 2
MC_LIB
CHPKNL
RTL
LOG_SYN
CELL_LIB
NETLST
LAY

FIG.11

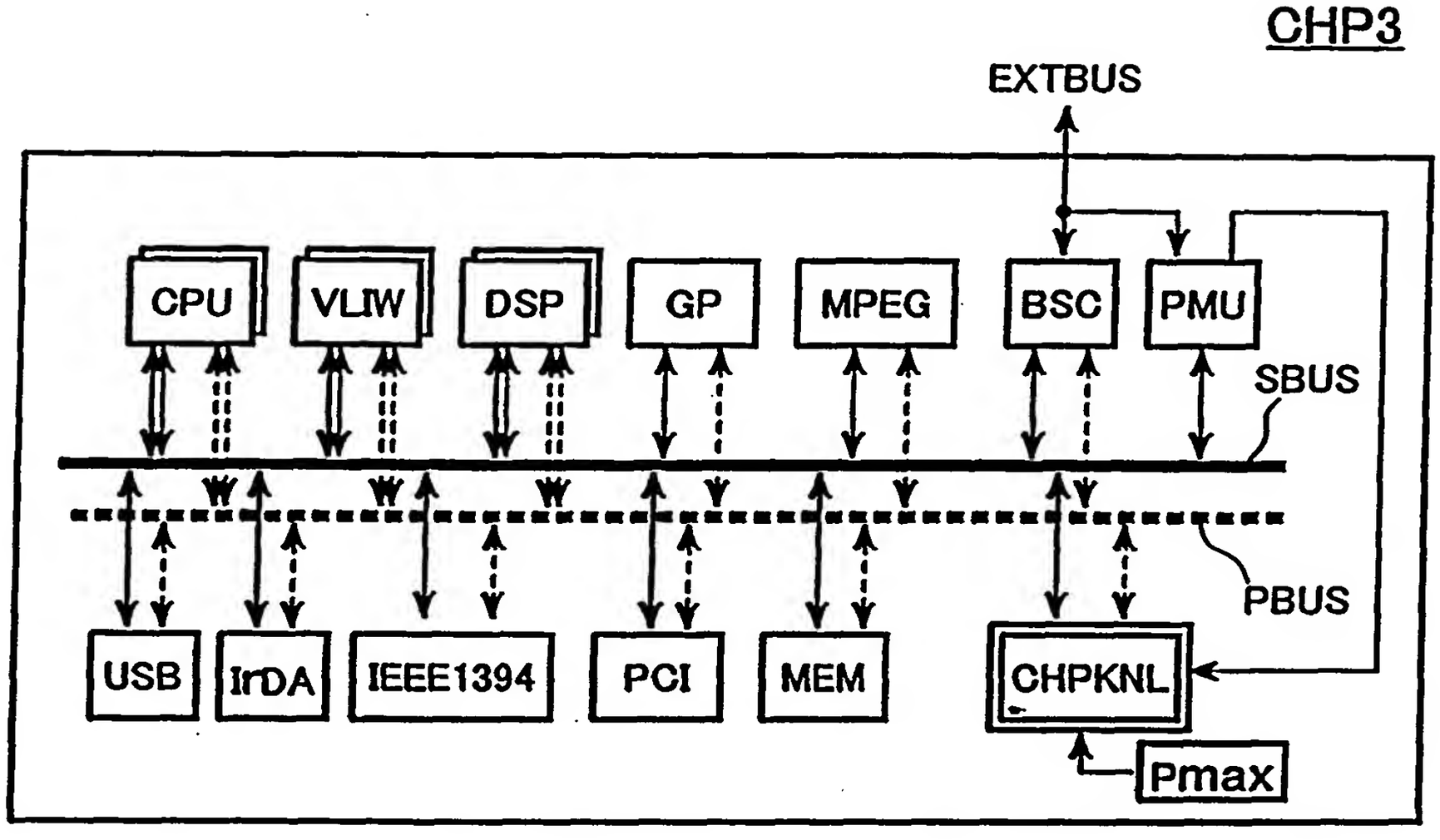
CHP3
EXTBUS
CPU
VLIW
DSP
GP
MPEG
BSC
PMU
SBUS
PBUS
USB
IrDA
IEEE1394
PCI
MEM
CHPKNL
Pmax

FIG.12

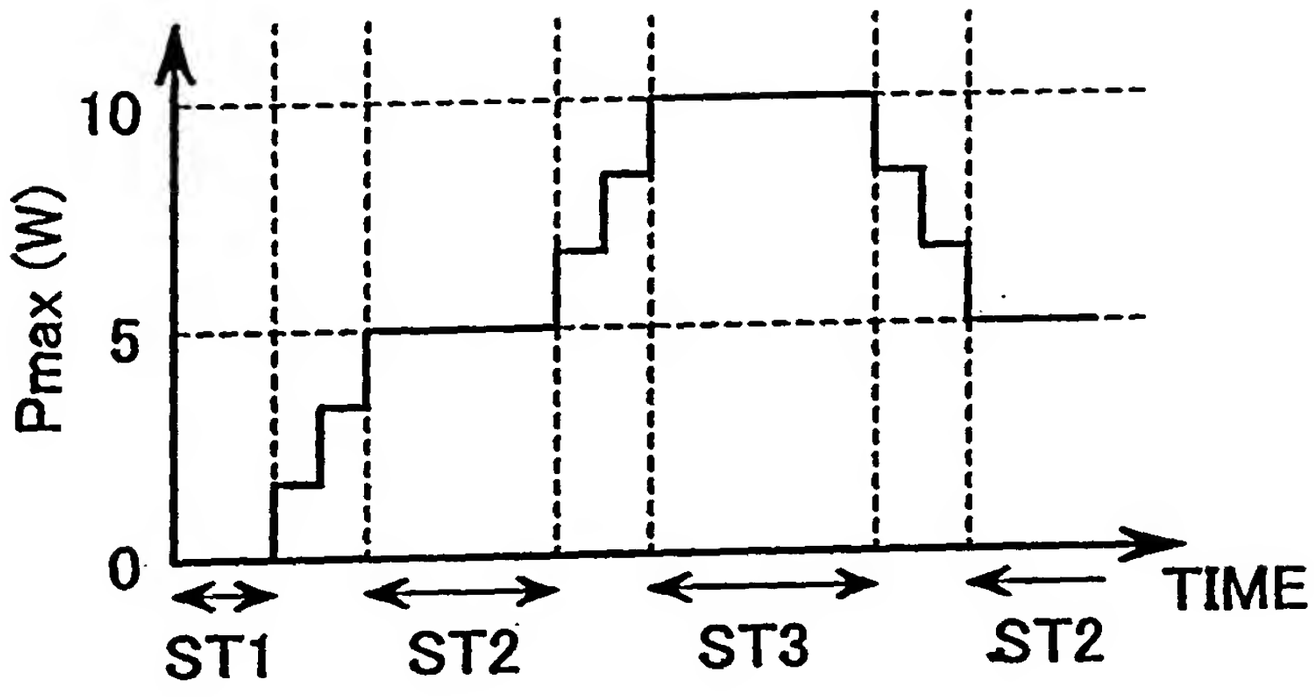

FIG.13